wherein said interpolation circuit includes a Q-times linear interpolation circuit and an R-times interpolation circuit composed of a plurality of transversal filters, said plurality containing a number of transversal filters equal to R;

A3

a sampling frequency of said analog-to-digital converter is set at a value approximately equal to a channel clock frequency; and

said digital signal output of said analog-to-digital converter is supplied to said digital phase-locked loop circuit to fetch a detection point voltage.--

REMARKS

Claims 1-31 remain in the application and have been amended hereby.

As will be noted from the Declaration, Applicant is a citizen and resident of Japan and this application originated there.

Accordingly, the amendments to the specification are made to place the application in idiomatic English, and the claims are amended to place them in better condition for examination.

An early and favorable examination on the merits is earnestly solicited.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT OF THE DISCLOSURE

The Abstract of the Disclosure has been amended as follows:

--A signal-processing circuit in which two-stage equalization is [carried out] performed by using first and second equalization circuits provided on [the] upstream and downstream sides from a [phase locked] phase-locked loop circuit, respectively, [is provided, wherein] the first equalization circuit on the upstream side [from the phase locked loop circuit is composed of] including a transversal filter[,] to minimize an equalization error caused by the first equalization circuit[, thereby stabilizing] and to stabilize the operation of the [phase locked] phase-locked loop circuit. Another signal-processing circuit including an analog-to-digital converter and a digital [phase locked] phase-locked loop circuit for receiving the output from the analog-to-digital converter[,] and a recording and playback apparatus using the [same] output are also provided, wherein the output from the analog-to-digital converter is input as the digital signal in the digital [phase locked] phase-locked loop circuit[,] to fetch a detection point voltage[, thereby] and for stabilizing [the operation of] the [phase locked] phase-locked loop circuit without [the need of provision of any] an analog circuit.--

IN THE CLAIMS

Claims 1-31 have been amended as follows:

--1. (Amended) A signal-processing circuit, comprising:

a [phase locked] phase-locked loop circuit for receiving playback data [obtained as a result of] resulting from analog-to-digital conversion of a playback signal from [a first] an equalization circuit[;],

wherein said first equalization circuit is composed of a transversal filter.

--2. (Amended) [A] The signal-processing circuit according to claim 1, wherein said [first] equalization circuit [is subjected to] includes means for performing adaptive equalization.

--3. (Amended) [A] The signal-processing circuit according to claim 1, wherein said equalization circuit comprises a first equalization circuit and further comprising a second equalization circuit provided on [the] a downstream side from [said phase locked] said phase-locked loop circuit[;], wherein

a sampling frequency of said first equalization circuit is made approximately equal to a channel clock frequency;

a [next time] subsequent transfer characteristic of said first equalization circuit is made equal to a product of a present [time] transfer characteristic of said first

equalization circuit and a present [time] transfer characteristic of said second equalization circuit; and

a [next time] subsequent transfer characteristic of said second equalization circuit is flattened.

--4. (Amended) [A] The signal-processing circuit according to claim 3, wherein [a] said transversal filter is used for each of said first equalization circuit and said second equalization circuit[,] to obtain [the next time] said subsequent transfer characteristic of said first equalization circuit by setting a [next time] subsequent tap coefficient of said first equalization circuit to a result of a convolutional integration of a present [time] tap coefficient of said first equalization circuit and a present [time] tap coefficient of said second equalization circuit.

--5. (Amended) [A] The signal-processing circuit according to claim 2, further comprising an adaptive equalization circuit provided on [the] a downstream side from said [phase locked] phase-locked loop circuit[;],

wherein said [first] equalization circuit is subjected to adaptive equalization by applying tap-coefficient-updating information output by said adaptive equalization circuit to a tap coefficient of said first equalization circuit in accordance with [the following equation]:

[next time] subsequent k-th tap coefficient = present [time] k-th tap coefficient + k-th tap-coefficient-updating

information.

--6. (Amended) [A] The signal-processing circuit according to claim 1, wherein said equalization circuit comprises a first equalization circuit and further comprising a second equalization circuit provided on [the] a downstream side from said [phase locked] phase-locked loop circuit[;], wherein

a sampling frequency of said first equalization circuit is set at a value higher than a channel clock frequency;

[the next time] a subsequent transfer characteristic of said first equalization circuit is divided into a portion in a first frequency band ["a"] being within a frequency band of said second equalization circuit and a portion in a second frequency band ["b"] being [out] outside of [a] said frequency band of said second equalization circuit;

[the] said portion of [the next time] said subsequent transfer characteristic of said first equalization circuit in [the] said first frequency band ["a"] is taken as a product of a portion of [the] said present time transfer characteristic of said first equalization circuit in [the] said first frequency band ["a"] and [the] said present transfer characteristic of said second equalization circuit, and [the] said portion of [the next time] said subsequent transfer characteristic of said first equalization circuit in [the] said second frequency band ["b"] is set to zero; and

[the next time] said subsequent transfer characteristic

of said second equalization circuit is flattened.

--7. (Amended) [A] The signal-processing circuit according to claim 6, wherein [a] said transversal filter is used for each of said first and said second equalization circuits[,] to determine [the next time] a subsequent tap coefficient of said first equalization circuit by [a manner of]:

obtaining a tap coefficient A of said first equalization circuit by subjecting [the] a present [time] tap coefficient of said first equalization circuit to fc/S1 thinning, where S1 denotes a sampling frequency of said first equalization circuit and fc denotes a channel [lock] clock frequency[,];

obtaining a convolution-integration result C in accordance with [an equation of] C = A * B, where [symbol]* denotes a convolution-integration operator and B denotes [the] a present [time] tap coefficient of said second equalization circuit[,];

obtaining a tap coefficient D by subjecting said convolution-integration result C to S1/fc-times interpolation[,]; and

taking [the tape] said tap coefficient D as [the next time] said subsequent tap coefficient of said first equalization circuit.

--8. (Amended) [A] The signal-processing circuit

according to claim 6, wherein [a] said transversal filter is used for each of said first and second equalization circuits[,] to determine [the next time] a subsequent tap coefficient of said first equalization circuit by [a manner of]:

obtaining a tap coefficient B of said second equalization circuit by subjecting [the] a present [time] tap coefficient of said second equalization circuit to fc/S1 thinning, where S1 denotes a sampling frequency of said first equalization circuit and fc denotes a channel [lock] clock frequency[,];

obtaining a convolution-integration result C in accordance with [an equation of] C = A * B, where [symbol]* denotes a convolution-integration operator and A denotes [the] a present [time] tap coefficient of said first equalization circuit[,]; and

taking [the] said convolution-integration result C as [the next time] said subsequent tap coefficient of said first equalization circuit.

--9. (Amended) [A] The signal-processing circuit according to claim 2, further comprising an adaptive equalization circuit provided on [the] a downstream side from said [phase locked] phase-locked loop circuit[;],

wherein said [first] equalization circuit is subjected to said adaptive equalization by [a manner of]:

making a sampling frequency S1 of said [first]

equalization circuit higher than a channel clock frequency fc;

obtaining a tap coefficient A by subjecting [the] a present [time] tap coefficient of said first equalization circuit to fc/S1 thinning;

calculating a [next time] subsequent value of said tap coefficient A in accordance with [the following equation]:

[next time] subsequent k-th value of tap coefficient A = present [time] k-th value of tap coefficient A + k-th tap-coefficient-updating information;

obtaining a tap coefficient B by subjecting said [next time] subsequent value of said tap coefficient A to S1/fc-times interpolation; and

setting said tap coefficient B to a [next time] subsequent tap coefficient of said first equalization circuit.

--10. (Amended) A signal-processing circuit, comprising:

an analog-to-digital converter for sampling a playback signal to convert said playback signal into a digital signal and for outputting said digital signal; and

a digital [phase locked] phase-locked loop circuit for receiving said digital signal from said analog-to-digital converter[;],

wherein said digital signal output by said analog-to-digital converter is supplied to said digital [phase locked] phase-locked loop circuit [so as] to fetch a detection-point voltage.

--11. (Amended) [A] The signal-processing circuit according to claim 10, further comprising [a first] an equalization circuit provided between said analog-to-digital converter and said [phase locked] phase-locked loop circuit[;].

wherein said [first] equalization circuit [is composed of] includes a digital transversal filter.

--12. (Amended) [A] The signal-processing circuit according to claim 11, further comprising an interpolation circuit provided between said [first] equalization circuit and said digital [phase locked] phase-locked loop circuit[;].

wherein said interpolation circuit is adapted to interpolate [sparse] separate pieces of sampling data with a period [close] approximately equal to a channel-clock period.

--13. (Amended) [A] The signal-processing circuit according to claim 12, wherein a sampling frequency of said analog-to-digital converter is [about] approximately equal to a channel-clock frequency.

--14. (Amended) [A] The signal-processing circuit according to claim 12, wherein said interpolation circuit includes a transversal filter for said interpolation and an R-times interpolation circuit; and

data is thinned at intervals of R taps of said transversal filter for said interpolation.

--15. (Amended) [A] The signal-processing circuit according to claim 14, wherein said R-times interpolation circuit is composed of R pieces of a plurality of transversal filters disposed in parallel [to each other].

--16. (Amended) [A] The signal-processing circuit according to claim 12, wherein said interpolation circuit includes a low-magnification interpolation circuit [composed of] that includes a transversal filter and a Q-times linear interpolation circuit provided on [the] a downstream side from said low-magnification interpolation circuit.

--17. (Amended) [A] The signal-processing circuit according to claim 16, wherein said Q-times linear interpolation circuit is composed of Q pieces of a plurality of interpolation circuits disposed in parallel [to each other].

--18. (Amended) [A] The signal-processing circuit according to claim 12, wherein said [phase locked] phase-locked loop circuit includes:

a data selector for receiving R X Q parallel trains of S X R X Q-times interpolation data from said interpolation circuit and selecting one of 0 [or] and 1 piece of said data closest to a detection point from said parallel trains of data for S > 1;

a detection point computing circuit for controlling

said data selector; and

a circuit for reporting one of 0 [or] said detection points and 1 said detection point.

--19. (Amended) [A] The signal-processing circuit according to claim 12, wherein said [phase locked] phase-locked loop circuit includes:

a data selector for receiving R X Q parallel trains of S X R X Q-times interpolation data from said interpolation circuit and selecting one of 0, 1, [or] and 2 pieces of said data closest to detection points from said parallel data for S $\leq$ 1;

a detection point computing circuit for controlling said data selector; and

a circuit for reporting one of 0, 1 [or] , and 2 said detection points.

--20. (Amended) [A] The signal-processing circuit according to claim 12, wherein said [phase locked] phase-locked loop circuit includes:

a plurality of data selectors [of the number of Dmax] for receiving P X R X Q parallel trains of S X R X Q-times interpolation data from said interpolation circuit and for selecting [the] a number of said data closest to [the] a plurality of maximum detection points from said parallel data, a quantity of data selectors in said plurality of data selectors being equal to Dmax;

a plurality of detection point computing circuits for controlling one of said plurality of data selectors [of the number of Dmax]; and

a circuit for reporting [the number] a plurality of detection points.

--21. (Amended) [A] The signal-processing circuit according to claim 11, wherein said [phase locked] phase-locked loop circuit includes:

[a] thinning period correcting means for absorbing frequency deviations while being updated in accordance with [an equation given below]:

$$d = d \pm \Delta d,$$

[where] wherein d denotes a thinning period[,] and Δd denotes a thinning period correction quantity;

[wherein the] and a value of [the] said thinning period correction quantity Δd given to said thinning period correcting means is changed in accordance with a response speed.

--22. (Amended) [A] The signal-processing circuit according to claim 11, wherein a buffer memory in which data output by said [phase locked] phase-locked loop circuit is stored and from which data is read with [another] a clock signal[,] is provided on [the] a downstream side from said [phase locked] phase-locked loop circuit.

--23. (Amended) [A] The signal-processing circuit according to claim 22, wherein said buffer memory has two memory banks; and

for S ≤ 1[, odd numbered] odd-numbered detection point data and [even numbered] even-numbered detection point data[, which are] output by said [phase locked] phase-locked loop circuit[,] are stored alternately into said two memory banks of said buffer memory.

--24. (Amended) [A] The signal-processing circuit according to claim 22, wherein said buffer memory has a plurality of memory banks [of the number of], a quantity of memory banks in said plurality of memory banks being equal to Dmax, [where] wherein Dmax is a maximum number of detection points simultaneously output by said phase locked loop circuit for receiving P X R X Q parallel trains of S X R X Q-times interpolation data[, and] Dmax is expressed by [an equation of]: Dmax = Int (P/S) + 1; and

[letting the] when a number of detection points reported by said phase locked loop circuit [be] is D [(D ≤ Dmax), the] and D is one of less than and equal to Dmax detection point data output by said [phase locked] phase-locked loop circuit are stored in said buffer memory having said D banks.

--25. (Amended) [A] The signal-processing circuit

according to claim 22, wherein [the] a frequency of said clock signal for reading data from said buffer memory is higher than [the] a frequency of a channel clock signal.

--26. (Amended) [A] The signal-processing circuit according to claim 25, wherein said buffer memory includes:

an empty-buffer detection circuit for outputting an empty-data signal to indicate that said buffer memory is empty[;],

wherein an operation of circuits provided at [the] a back of said empty-buffer detection circuit is stopped based on [the basis of] said empty-data signal.

--27. (Amended) [A] The signal-processing circuit according to claim 22, further comprising a [voltage controlled] voltage-controlled oscillator for generating said clock signal for reading said data from said buffer memory.

--28. (Amended) [A] The signal-processing circuit according to claim 27, wherein an oscillation frequency of said [voltage controlled] voltage-controlled oscillator is controlled [so that neither] to prevent an empty-data state [nor] and a data overflow [occurs] in said buffer memory.

--29. (Amended) [A] The signal-processing circuit according to claim 28, wherein said [voltage controlled] voltage-controlled oscillator is subjected to feedback control

[so] such that a read address to read [out] said data from said buffer memory and a write address to write said data into said buffer memory satisfy [the following equation]:

(write address - read address) = a maximum difference.

--30. (Amended) A recording and playback apparatus having a recording system and a playback system each employing a signal-processing circuit, each of said signal-processing [circuit employed in said playback system] circuits comprising:

a first equalization circuit;

a [phase locked] phase-locked loop circuit for receiving playback data obtained as a result of analog-to-digital conversion of a playback signal [from] by said first equalization circuit; and

a second equalization circuit provided on [the] a downstream side from said [phase locked] phase-locked loop circuit[;].

wherein each of said first and said second equalization circuits is composed of a transversal filter;

a sampling frequency of said first equalization circuit is set at a value approximately equal to a channel clock frequency;

a [next time] subsequent transfer characteristic of said first equalization circuit is made equal to a product of a present [time] transfer characteristic of said first equalization circuit and a present [time] transfer

characteristic of said second equalization circuit; and

a [next time] subsequent transfer characteristic of said second equalization circuit is flattened.

--31. (Amended) A recording and playback apparatus including a recording system and a playback system each employing a signal-processing circuit, each of said signal-processing [circuit employed in said playback system] circuits comprising:

an analog-to-digital converter for sampling a playback signal to convert said playback signal into a digital signal;

a digital [phase locked] phase-locked loop circuit for receiving said digital signal from said analog-to-digital converter;

[a first] an equalization circuit composed of a digital transversal filter, said [first] equalization circuit being provided between said analog-to-digital converter and said [phase locked] phase-locked loop circuit; and

an interpolation circuit for interpolating [sparse] separate pieces of sampling data with a period [close] approximately equal to a channel clock period, said interpolation circuit being provided between said [first] equalization circuit and said digital [phase locked] phase-locked loop circuit[;],

wherein said interpolation circuit includes a Q-times linear interpolation circuit and an R-times interpolation circuit composed of a plurality of transversal filters [of the

number of] , said plurality containing a number of transversal filters equal to R[.];

a sampling frequency of said [ADC] analog-to-digital converter is set at a value approximately equal to a channel clock frequency; and

said digital signal output [by] of said analog-to-digital converter is supplied to said digital [phase locked] phase-locked loop circuit [so as] to fetch a detection point voltage.--